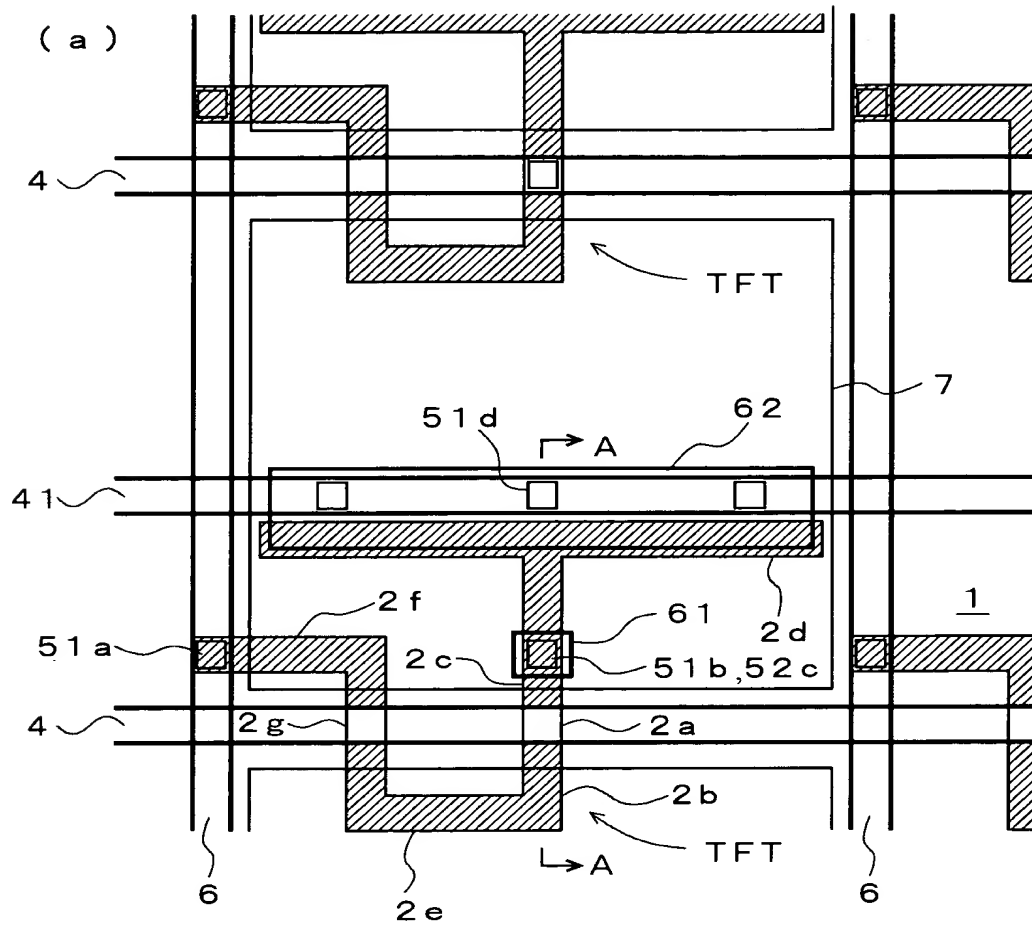


FIG. 1



(b)

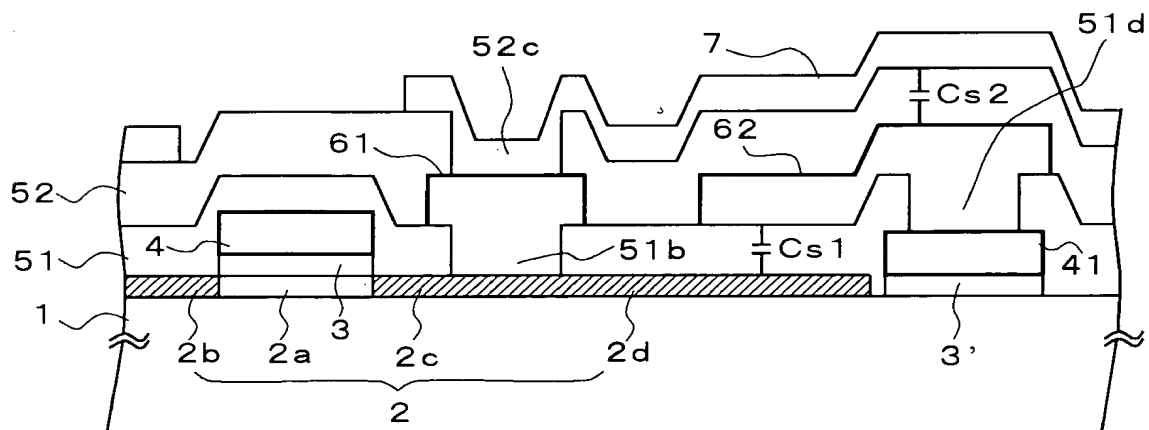
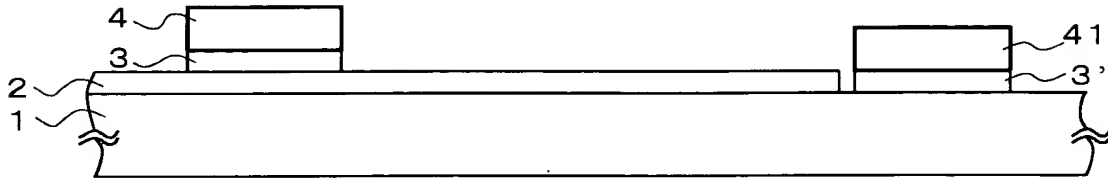
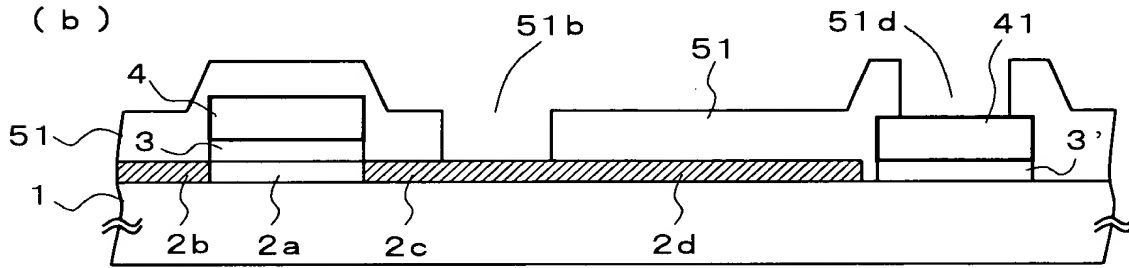


FIG. 2

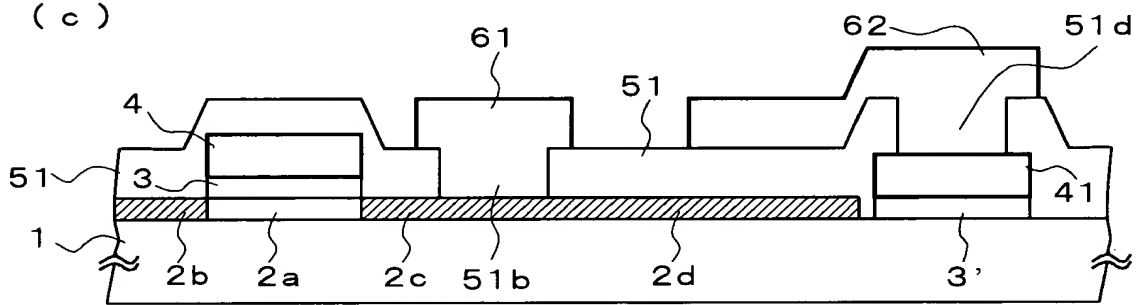
(a)



(b)



(c)



(d)

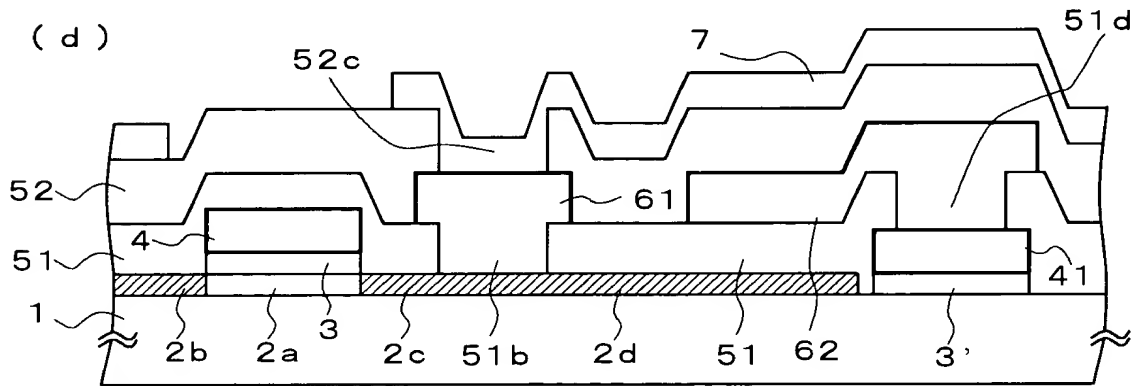
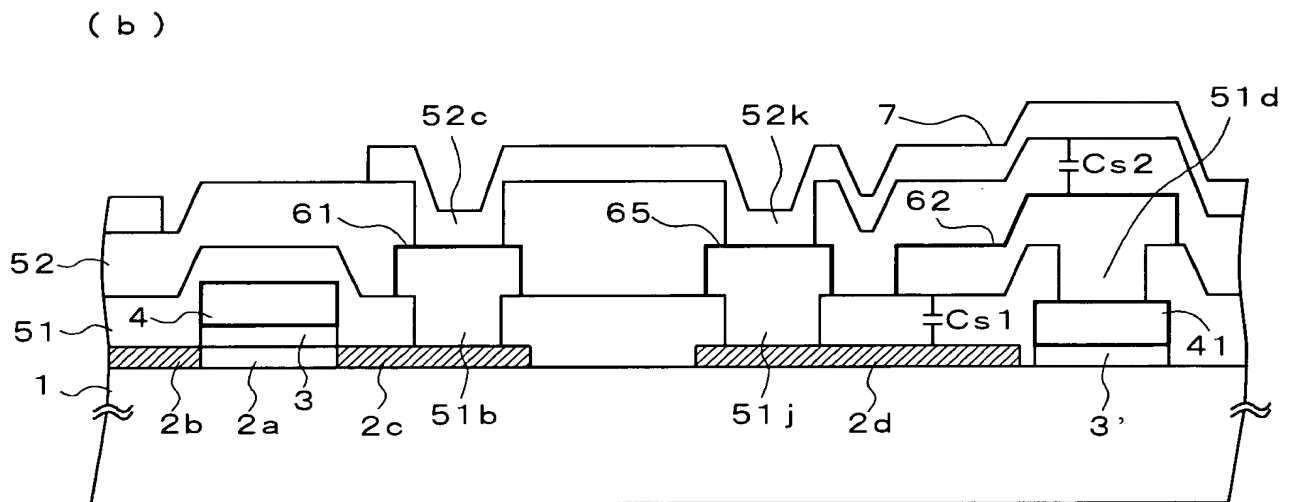
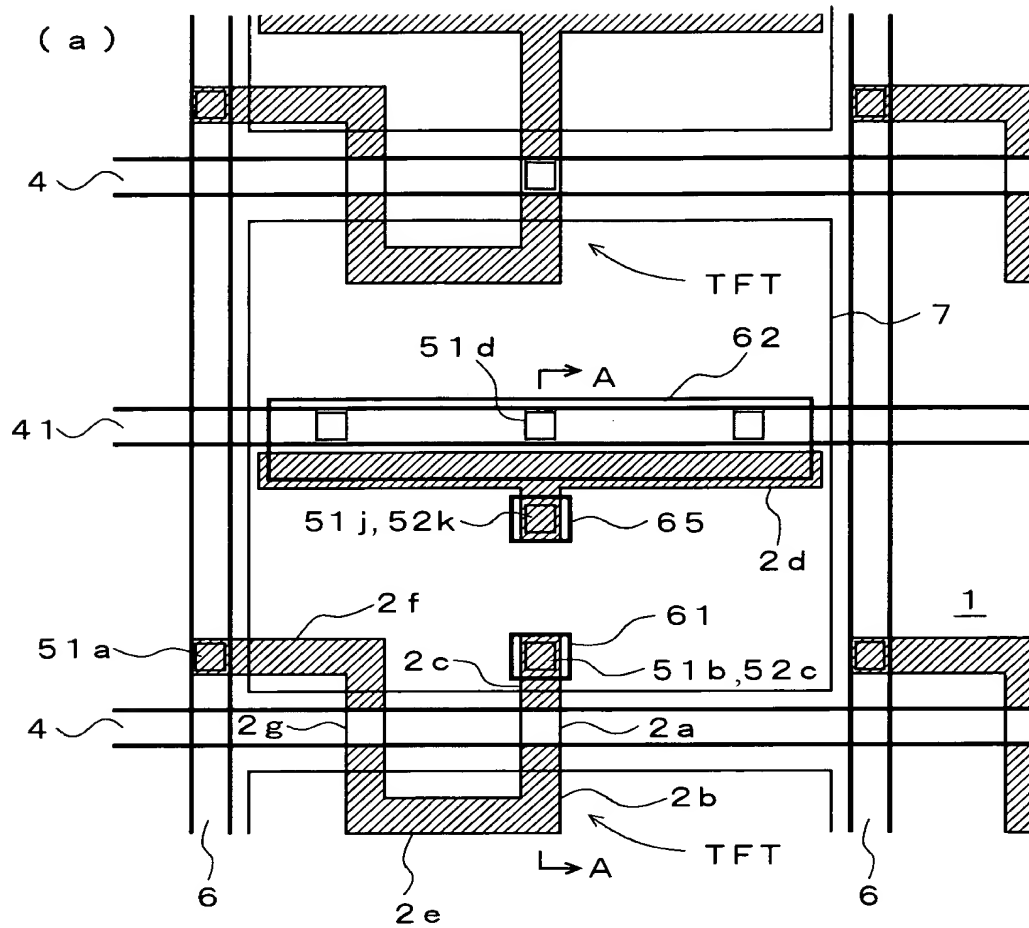


FIG. 3



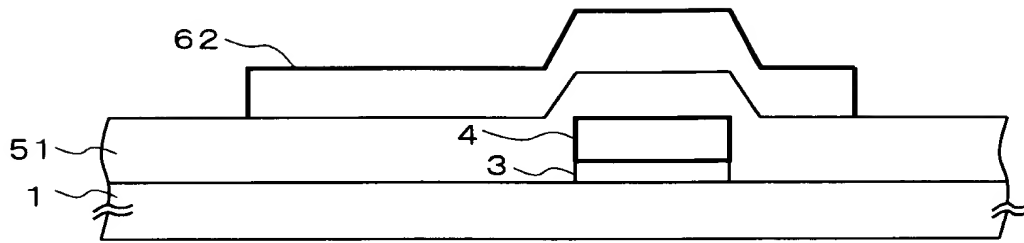
(a)

Diagram (a) is a plan view of a semiconductor device. It shows two TFTs (51a and 51b) and various interconnects. The TFTs are labeled 51a and 51b, 52c. The interconnects are labeled 2a, 2b, 2c, 2e, 2f, 2g, 4a, 4b, 6, 7, 8. The device is divided into two main sections by a vertical line. The left section contains TFT 51a and the right section contains TFT 51b. The interconnects are arranged in a grid-like pattern. The labels 2a, 2b, 2c, 2e, 2f, 2g, 4a, 4b, 6, 7, 8 are used to identify specific components. The labels 51a and 51b, 52c are used to identify the TFTs. The labels 2a, 2b, 2c, 2e, 2f, 2g, 4a, 4b, 6, 7, 8 are used to identify the interconnects. The labels 51a and 51b, 52c are used to identify the TFTs. The labels 2a, 2b, 2c, 2e, 2f, 2g, 4a, 4b, 6, 7, 8 are used to identify the interconnects.

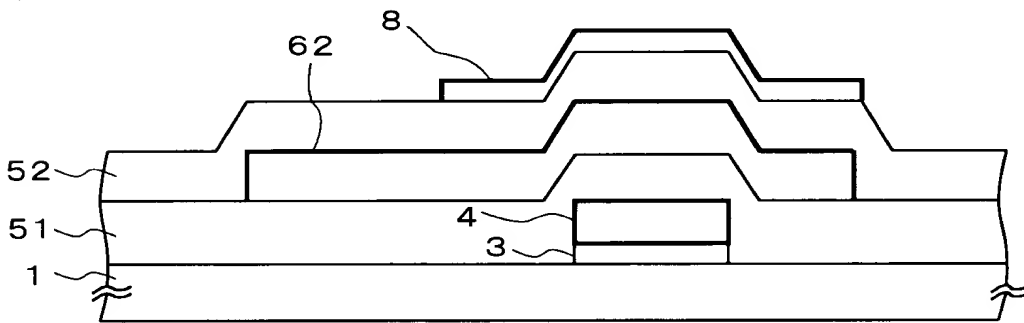
[illegible]

FIG. 5

(a)



(b)



(c)

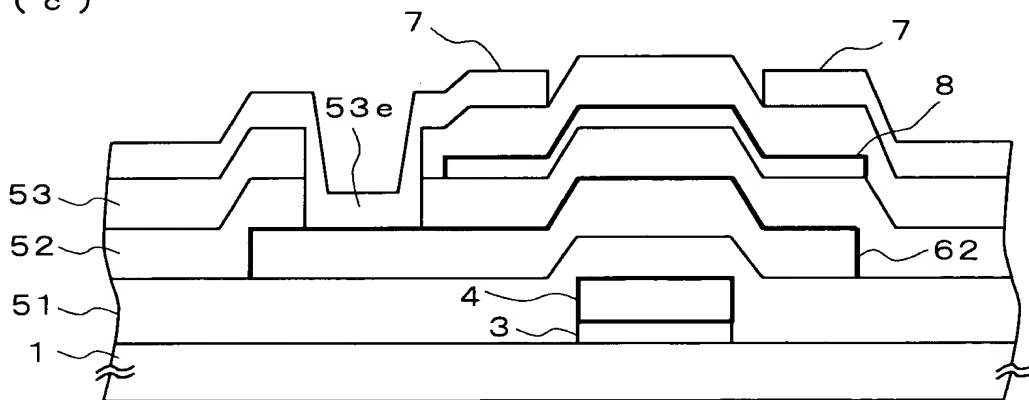


FIG. 6

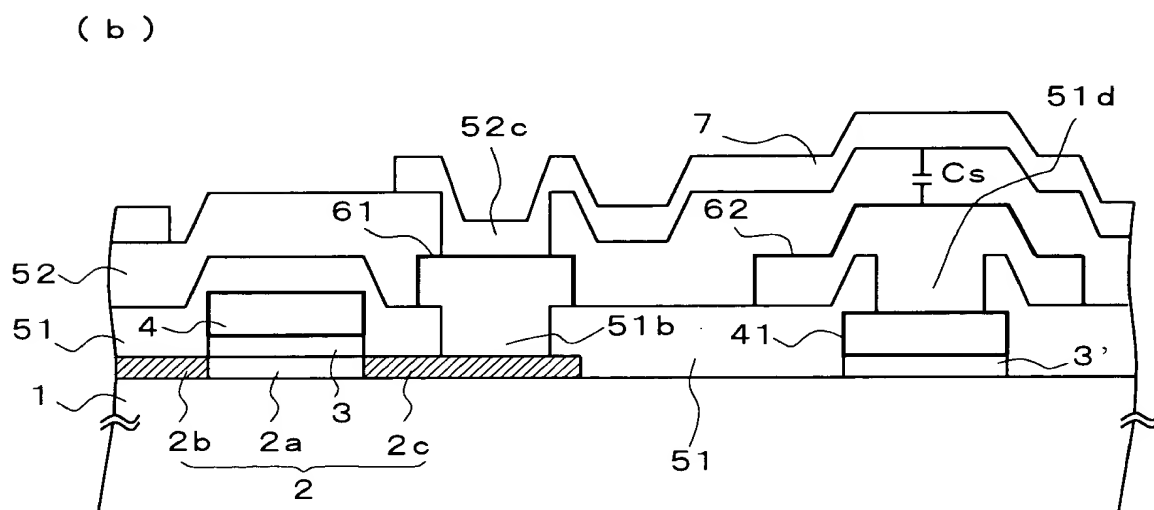
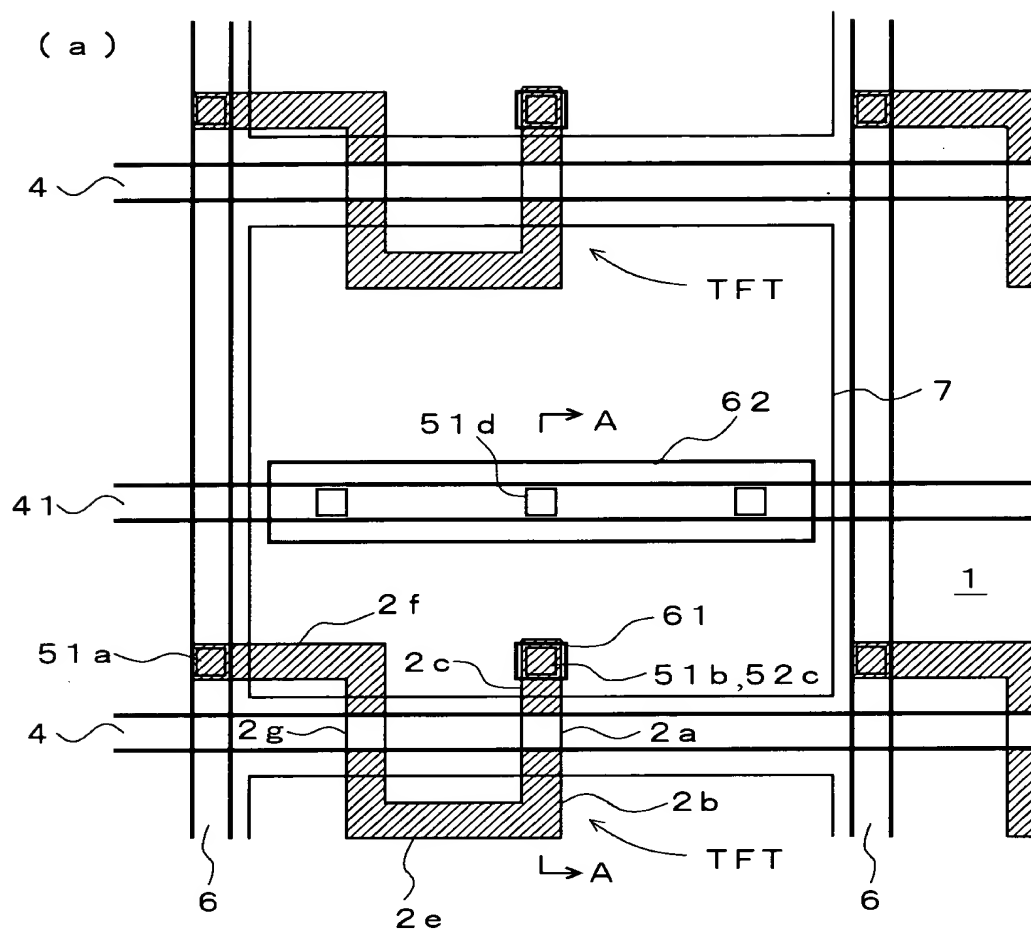


FIG. 7

